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Engineering Note

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Project:	DFEA
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Subject:	Framing and Control bits in the LVDS links to the DFEA

All **Orange** and **Blue**[1] LVDS links going from the MIXER to the DFEA should look like this:

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																									XOR_FX	FX	0	1
																									XOR_SG	SG	0	2
																									XOR_RST	RST	0	3
				CFT/CPS Axial Singlets																					XOR_B396	B396	0	4
																									XOR_L1A	L1A	0	5
																									XOR_TM	TM	0	6
																									0	0	1	7

RST	CFT Reset, active high	XOR_RST	logical XOR of all CFT reset bits received on a MIXER board
L1A	L1_ACCEPT, active high	XOR_L1A	logical XOR of all L1_ACCEPT bits received on a MIXER board
SG	Sync Gap, active high	XOR_SG	logical XOR of all SYNC_GAP bits received on a MIXER board
B396	Beam 396 marker, active high	XOR_B396	logical XOR of all BEAM_396 bits received on a MIXER board
FX	First Crossing, active high	XOR_FX	logical XOR of all FIRST_CROSSING bits received on a MIXER board
TM	Test Mode, active high	XOR_TM	logical XOR of all TEST_MODE bits received on a MIXER board

Along with the seven control bits, there are 7 XOR bits. The purpose of the XOR bits is to inform the DFEA if the control bits received on a MIXER board do not agree. For example, if one of the AFE boards feeding into a MIXER board does not assert the CFT_RESET bit but the other AFE boards do, then the MIXER board should set the RST bit and also the XOR_RST bit when sending data to the DFEA.

Note: The control bits contained inside a frame are assumed to apply to the singlet data in that frame.

[1] The rest of the links going to the DFEA need only to have the End of Frame marker in the LSb position as shown above.

- When a 21-bit wide LVDS link transmitter is connected to a 28-bit wide LVDS link receiver, the 21 valid bits are scattered across the 28 receiver output pins. Below is a table showing the mapping between 21-bit and 28-bit LVDS channel links.

21-bit link TX	28-bit link RX
D0	Q0
D1	Q1
D2	Q2
D3	Q3
D4	Q4
X	Q5
D5	Q6
D6	Q7
D7	Q8
D8	Q9
X	Q10
X	Q11
D9	Q12
D10	Q13
D11	Q14
D12	Q15
X	Q16
X	Q17
D13	Q18
D14	Q19
D15	Q20
D16	Q21
D17	Q22
X	Q23
D18	Q24
D19	Q25
D20	Q26
X	Q27

D[20..0] → | 21-bit LVDS TX | CLK/CLK* Y0P/Y0M Y1P/Y1M Y2P/Y2M ⟷ CLK/CLK* A0M/A0P A1M/A1P A2M/A2P A3M/A3P | 28-bit LVDS TX | → Q[27..0]

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